REMARKS

Claims 1-36 are pending in the application. Claims 1, 13, and 25 are independent claims. Claims 1-36 stand rejected.

As an initial matter, Applicants submit that the finality of the rejection is clearly improper. The propriety of final rejections is described in the MPEP § 706.7(a). As that section dictates:

> Under present practice, second or any subsequent actions on the merits shall be final, except where the examiner introduces a new ground of rejection that is neither necessitated by applicant's amendment of the claims, nor based on information submitted in an information disclosure statement filed during the period set forth in **37 CFR 1.97(c)** with the fee set forth in **37 CFR 1.17(p)**.

Id. Not only was the rejection not necessitate by Applicants amendments, but the examiner apparently did not consider the arguments because they are "moot in view of the new ground of rejection." Action p. 8. Since the finality of the rejection was neither necessitate by the Applicants amendments nor by a reference submitted in an IDS, Applicants respectfully request that the examiner reconsider and withdraw the finality of the rejection.

Claims 1, 13, 25 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

While Applicants do not necessarily agree that the claims are indefinite, Applicants have amended the claims in order to address the points made by the examiner to expedite prosecution.

Applicants submit that the claims, particularly as amended, are definite and request reconsideration of the rejection.

Claims 1-36 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kimmel et al., Patent No. 6,105,053 (hereafter Kimmel) in view of Kaushik et al., Patent No. 7,191,349 (hereafter Kaushik).

Regarding claim 1, the examiner asserts that Kimmel teaches:

> selecting a first cluster from at least two clusters (Fig 1 A: all JP that routes to the same shared memory corresponds to a cluster. For example, ***JPO and JP1 make up one cluster***.),

Action p. 7. The examiner cites Kimmel as teaching the two job processors (JP0 and JP1) make up one cluster. Applicants agree that a cluster comprises more than one processor. However, next the examiner maintains that:

> each cluster having an associated priority indicator, where the selected cluster is selected as a function of its priority indicator(Col 9, lines 28-38: each node on level 1, which corresponds to a cluster, gets its own run queue. Col 6, lines 10-15, 54-61: each thread group has its own priorities. ***Each queue in all of the node levels contains the thread groups and their associated priorities***. Thus each node on level 1 will have priority values associated with it. Col 13, line 40-Col 14, line 27; Col 15, line1, Col 16, lines 35-47: load value for each node can be measure using priorities found in its queues, which can then be used by the scheduler perform load balancing among any nodes at any level, thus selecting a node to execute a thread group when other nodes are overloaded);

Action p. 7. As this excerpt from the action makes clear. The examiner finds that priority indicator in Kimmel is associated with the thread, and not with the cluster. However the claim clearly recites the opposite proposition, i.e., each cluster has an associated priority indicator. This distinction becomes more apparent when considered in the context of the remaining claim language. For example, the examiner goes on to argue that Kimmel teaches:

> selecting a first processor from the cluster, the cluster comprising at least two processors (Fig 1B, node 110 corresponds to a cluster, unit 100 and 101 are processors.), ***each processor having an associated priority indicator***, where the selected processor is selected as a function of its priority indicator (Col 13, line 40-Col 14, line 27; Col 15, line 1, Col 16, lines 35-47);

Action p. 7. Here while the claim recites that the processors have an associated priority indicator, where that priority indicator is used to select a processor, the examiner again cites to the thread group priority indicator that is used in Kimmel to schedule and balance the execution of threads. That priority indicator is then used in the claims to associate the processor with a set of computer-readable instructions, e.g., a thread. For example, claim 1 recites: associating the first processor with the first set of computer readable instructions. Kimmel teaches the opposite.

The examiner maintains the above analysis from the previous action, but attempts to cure the lack of teaching of Kimmel by citing Kaushik. Kaushik does not teach the elements missing from Kimmel. The examiner maintains that Kaushik teaches:

> However, Kaushik teaches a processor have a priority indicator directly indicating the priority of the processor. Furthermore, the priority of the processor is the function of the priorities of tasks that runs on the processor for the purpose of letting the priority of tasks running on the processor to represent the priority of the processor itself (Column 3, lines 13-25).

Action, p. 4. But Kaushik actually teaches:

> The advanced programmable interrupt controller (APIC) architecture allows for the delivery of a device interrupt to a processor that is operating at the lowest priority among a set of target processors. This processor priority is determined via the contents of the task priority register for those processors. This feature is based on the concept that the priority that a processor is presently running at represents the criticality of the task being performed. The higher the task priority, the less desirable it would be to interrupt that processor as there can be an undesirable impact on overall performance. Furthermore, by directing an interrupt to the processor operating at the lowest priority in the system would provide a better chance that the interrupt might be serviced with a minimal amount of wait time.

Kaushik says nothing of cluster priority. Moreover, the priority of Kaushik is different from the claimed priority. Kaushik teaches that a task priority register is used to determine which processor should not be interrupted. As such Kaushik does not cure the defect of Kimmel. In particular the combination does not teach:

> selecting the first processor from the cluster, the cluster comprising at least one other processor, each processor having an associated priority indicator, where the selected first processor is selected as a function of its priority indicator indicating the priority of the first processor; and
>
> associating the first processor with the first set of computer-readable instructions.

For at least the foregoing reason, claim 1 patentably defines over Kimmel in view of Kaushik. Inasmuch as claims 2-12 incorporate the same limitations by virtue of their

dependence from claim 1, Applicants submit that they also patentably define over Kimmel in view of Kaushik.

Regarding claims 13-24, the examiner provided no additional analysis and instead reiterated the analysis of claim 1:

> As per claims 13-24, they are computer-readable medium claims of claims 1-12. Therefore, they are rejected as claims 1-12 above.

Action p. 8. Accordingly, for at least the same reasons as are indicated above, Applicants submit that claims 13-24 patentably define over Kimmel in view of Kaushik.

In addition, Applicants have amended claim 13 to recite:

> removing the first processor from the association with the first set of computer-readable instructions in the reverse order that it was associated with the first set of computer-readable instructions.

This limitation further patentably defines over Kimmel in view of Kaushik.

Similarly with respect to claims 25-36, the examiner again merely reiterated the claim 1 analysis:

> As per claims 25-36, they are system claims of claims 1-12. Therefore, they are rejected as claims 1-12 above.

Action p. 8. Accordingly, for at least the same reasons as are indicated above, Applicants submit that claims 25-36 patentably define over Kimmel.

CONCLUSION

In the view of the foregoing amendments and remarks, Applicants respectfully submit that the present application is in condition for allowance. Reconsideration of the application and an early Notice of Allowance are respectfully requested. In the event that the Examiner cannot allow the application for any reason, the Examiner is encouraged to contact Applicants' representative.

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